Amendments to the Drawings:

Formal drawings are submitted herewith which incorporate the changes required by the Examiner. Approval by the Examiner is respectfully requested.

Attachments: Replacement Figures 1-6

REMARKS

Claims 1-12 are rejected. Claim 7 has been amended. Claims 1-12 are presently pending in the application. Favorable reconsideration of the application in view of the following remarks is respectfully requested.

The basis for the amendment of claim 7 is found in claim 1 as originally filed.

Rejection of Claims 1-12 Under 35 U.S.C. §102(e):

The Examiner has rejected Claims 1-12 under 35 U.S.C. 102(e) as being anticipated by Huang, XiaoYang et al. (US 2005/0083284 A 1), indicating that, regarding Claim 1, Huang, Xiao-Yang teaches a method of driving an active matrix cholesteric liquid crystal display that includes a matrix of data and select lines and an array of pixels connected to the data and select lines through active switching elements, a pixel being capable of producing two or more gray levels, comprising: a) providing a select voltage and a plurality of data voltages; and b) during a pixel writing cycle, applying the select voltage and the data voltages to the select and data lines of the display to produce only three pixel voltage levels 0, +U and -U, having respective duty cycles and controlling the duty cycles of the pixel voltage levels to determine the gray levels of the pixels, gray scale is represented by amplitude modulation, and also teaches gray scale is implemented with determination of driving voltage, pulse width, and frame rate control (duty cycle)), and wherein the average voltage applied to a pixel during the pixel writing cycle is zero. Regarding Claim 7, the Examiner indicates that Huang, Xiao-Yang teaches an active matrix cholesteric liquid crystal display that includes a matrix of data and select lines and an array of pixels connected to the data and select lines through active switching elements, a pixel being capable of producing two or more gray levels, comprising: a) providing a select voltage and a plurality of data voltages; and b) during a pixel writing cycle, applying the select voltage and the data voltages to the select and data lines of the display to produce only three pixel voltage levels 0, +U and -U, having respective duty cycles and controlling the duty cycles of the pixel voltage levels to determine the gray levels of the pixels, gray scale is represented by amplitude modulation, and also teaches gray scale is implemented with determination of driving voltage, pulse width, and frame rate control (duty cycle)), and wherein the average voltage applied to a pixel during the pixel writing cycle is zero.

Huang discloses a graphics controller for a color display system having a bistable liquid crystal display (LCD) for displaying a plurality of pixels arranged in a matrix, which includes a memory device and a generating. In an exemplary case, the bistable LCD is a Cholesteric LCD and, preferably, the generating device has a first mode of operation in which the data corresponding to the pixels is generated for each corresponding pixel and a second mode of operation in which no data is generated. The generating device switches from the first operating mode to the second operating mode when all of the status bits for all of the pixels are zeros.

The present invention relates to a display and a method of driving an active matrix cholesteric liquid crystal display that includes a matrix of data and select lines and an array of pixels connected to the data and select lines through active switching elements, a pixel being capable of producing two or more gray levels, comprising a) providing a select voltage and a plurality of data voltages; and b) during a pixel writing cycle, applying the select voltage and the data voltages to the select and data lines of the display to produce only three pixel voltage levels 0, +U and –U, having respective duty cycles and controlling the duty cycles of the pixel voltage levels to determine the gray levels of the pixels, and wherein the average voltage applied to a pixel during the pixel writing cycle is zero.

A claim is anticipated under 102(e) only if each and every element as set forth in the claim is found, either expressly or inherently, in a single prior art reference. Verdegaal Bros. V. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Review of Fig. 5a of the reference provides five voltage levels: +30, -30, zero, +40 and –40, specifically at BP, p11, p12, and p22 of Fig. 5a. The present invention claims applying the select voltage and the data voltages to the select and data lines of the display to produce only three pixel voltage levels 0, +U and –U. Utilizing the terms of Huang, the present invention is limited to three pixel voltage levels: if U is 30, the three pixel voltage levels are +30, -30, zero; if U is 40, the three pixel voltage levels are +40, -40, zero. Additional detail relating to the differences between Huang and the present invention are contained at pg. 2, lines 10-17. This section discusses US 2001/050666 A1, claiming priority to US 60/200,001, from which the reference cited by the Examiner claims priority. As a result, the discussion beginning on

pg. 2, line 10 – pg. 3, line 11, and including Fig. 2 of the present invention, also applies directly to the presently cited reference. Therefore, the reference fails to teach applying the select voltage and the data voltages to the select and data lines of the display to produce only three pixel voltage levels.

Claims 2-6 benefit from dependence on claim 1, which, as discussed above, Applicants believe is novel in light of the reference.

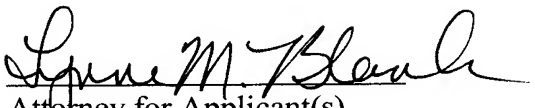
Claims 8-12 benefit from dependence on claim 7 which, as discussed above, Applicants believe is novel in light of the reference.

Prior Art:

The Examiner also notes Doane; J. William et al. (US 6518944 B 1), made of record and not relied upon but considered pertinent to applicant's disclosure, which relates to combined cholesteric liquid crystal display and solar cell assembly device. However, this reference also fails to teach applying the select voltage and the data voltages to the select and data lines of the display to produce only three pixel voltage levels 0, +U and –U.

It is believed that the foregoing is a complete response to the Office Action and that the claims are in condition for allowance. Favorable reconsideration and early passage to issue is therefore earnestly solicited.

Respectfully submitted,



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Enclosures: Replacement Figures 1-6
Copies of Formal Drawings

If the Examiner is unable to reach the Applicant(s) Attorney at the telephone number provided, the Examiner is requested to communicate with Eastman Kodak Company Patent Operations at (585) 477-4656.